A 6b Stochastic Flash Analog-to-Digital Converter Without Calibration or Reference Ladder

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***Abstract*—A 6-bit stochastic flash ADC is presented. By connecting many comparators in parallel, a reference ladder is avoided by allowing random offset to set individual trip points. The ADC transfer function is the cumulative density function of comparator offset. A technique is proposed to improve transfer function linearity by 8.5 dB. A test chip, fabricated in 0.18μm CMOS, achieves ENOB over 4.9b up to 18MS/s with 900mV supply and comparator offset standard deviation of 140mV. Comparators are digital cells to allow automated synthesis. Total core power consumption when f_S = 8 MHz is 631μW.**

I. Introduction

As CMOS designs are scaled to smaller technology nodes, many benefits arise as well as challenges. There are benefits in speed and power due to decreased capacitance and lower supply voltage, yet reduction in intrinsic device gain and lower supply voltage make it difficult to migrate previous analog designs to smaller scaled processes, and new circuit techniques are required. The technique presented in this paper will be discussed in the context of the scaling of flash and subranging data converters to future digital CMOS processes.

All comparators have some input-referred offset due to random device mismatch. In a flash ADC, minimizing comparator offset is critical to the overall accuracy of the converter. In a subranging flash ADC, it is the offsets of the subrange comparators that are most critical. In both regimes, the critical comparators must be accurate to within the overall desired accuracy of the converter. This requires that each comparator consume a large area footprint in an effort to reduce device mismatch, or implement offset-canceling circuit techniques such as output offset storage (OOS) as described in [1]. The latter technique requires storing offset values on capacitors at the output of gain stages. This leads to increased power consumption, especially since in some cases multiple cascaded gain stages are required [2]. Instead of suppressing comparator offset, it is possible to use the random nature of the offset as part of a stochastic ADC.

Flash ADCs use some sort of reference ladder to generate the comparator trip points that correspond to each digital code. First proposed in [3], a stochastic ADC uses device mismatch to generate these trip-points. Consider a large array of identically drawn comparators, each with a random input-referred offset. Individual offsets are unknown, as they are random, but the overall offset distribution can be defined by its probability density function (PDF). If all of these comparators are connected in parallel, i.e. their inputs are all connected as in Fig. 1(b), and a linear ramp is applied at the input, a plot of the number of comparators that evaluate high against the input will follow the cumulative density function (CDF) which is merely the integral of the PDF as depicted in Fig. 1. It has been proposed in [4] that by determining the offset of each comparator, it is possible to choose comparators with offsets that correspond to a desired transfer function. This solution requires a computationally expensive foreground calibration to generate a transfer function. If comparator offset follows a Gaussian distribution or other distribution with a near linear CDF, then the CDF can be used *as* the transfer function without calibration.

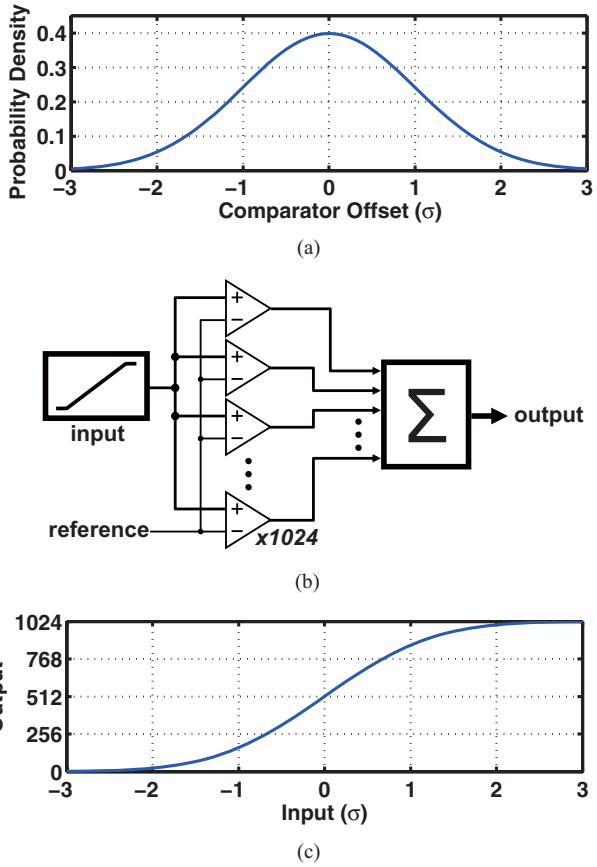

Fig. 1. a) Probability density function of comparator offset in terms of standard deviation, σ, assuming Gaussian distribution. b) 1024 comparators connected in parallel with a single, fixed reference and a ramp input c) Output of 1024 comparators with ramp input in terms of σ.

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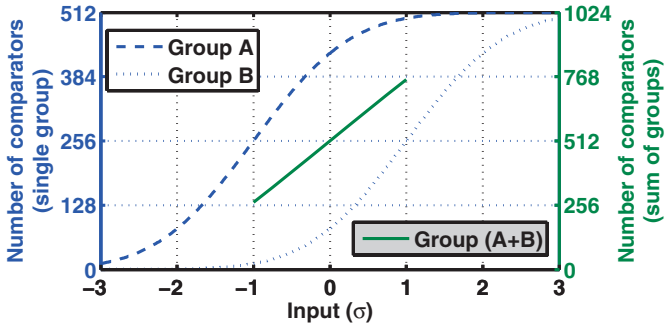


Fig. 2. Transfer functions for two groups of parallel comparators with fixed references of $-\sigma$ and $+\sigma$ for groups A and B, respectively. The sum of these groups has higher linearity over the range $-\sigma$ and $+\sigma$.

II. Circuit Implementation

A. System Level Consideration

The transfer function of a stochastic ADC implemented as a single group of comparators will be related to the CDF of comparator offset. Given that comparator offset is Gaussian, the CDF is somewhat linear about the mean; however, the nonlinearity that does exist will lead to distortion in the output. A straightforward solution to correct this nonlinearity is to scale the output by the inverse function of the CDF. This could be implemented as a lookup table and can theoretically achieve very high linearity, but requires startup calibration to determine the lookup table values [5].

Another solution is to benefit from the specific shape of a Gaussian CDF. If the fixed reference for a single group of parallel comparators is equal to a value of x, then the value of the input corresponding to half of the comparators evaluating high will also be x. This provides a way to influence the effective mean of the comparator offset distribution. If two groups of parallel comparators are given differing values for their fixed references, then the input to output transfer functions for each group will be separated by the difference between references, as illustrated in Fig. 2. If the CDFs are separated by about two standard deviations, the sum of the CDFs will have a linear region between the two references. Although this does not yield perfect linearity, it can be implemented with a single digital addition. Because of its simplicity, this is what was implemented for the test chip.

B. Comparator Design

To verify the claim that comparator offset is Gaussian, the test chip contains as many comparators as possible to increase statistical significance. Since we also want to obtain measurement results for a stochastic flash ADC, the comparators are separated into two groups of 3840 comparators each, with a single reference per group. It is not likely that such a large number of comparators would be implemented in a realistic ADC implementation, therefore the two groups are then subdivided into 20 subgroups that can be enabled and disabled independently of one another. The comparator schematic can be seen in Fig. 3. The comparator is followed by

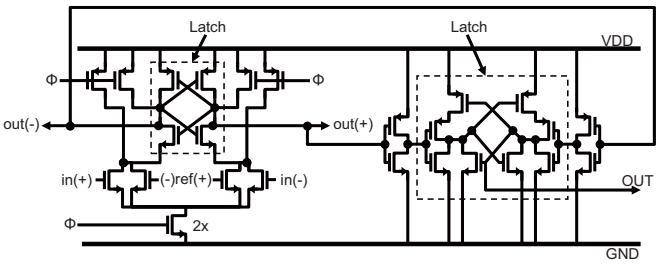


Fig. 3. Schematic of comparator with a secondary latch to maintain digital output when comparator is reset. All transistor sizes are W/L = 0.22μm/0.18μm (the minimum allowed in this 0.18μm process) with the exception of the indicated "2x" transistor which is W/L = 0.42μm/0.18μm.

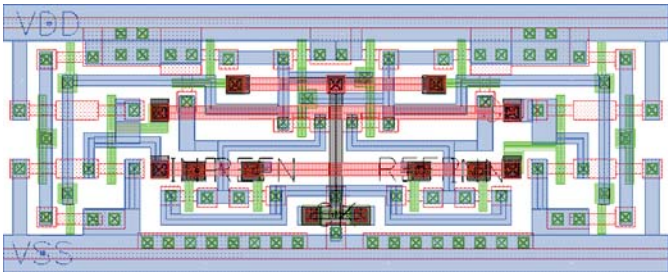
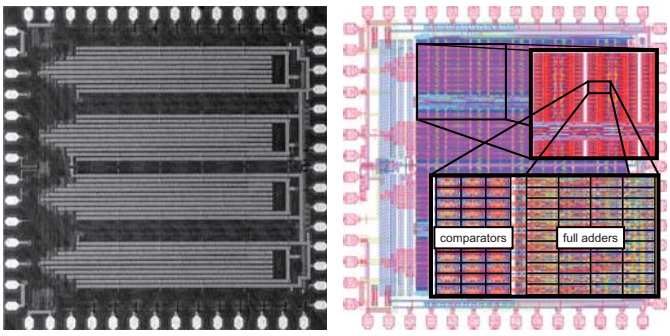


Fig. 4. Layout of comparator and secondary latch. Minimum sized devices are used and supply rail pitch matches digital library cells to allow for fully automated synthesis. Cell dimensions are 14.55μm by 5.84μm.



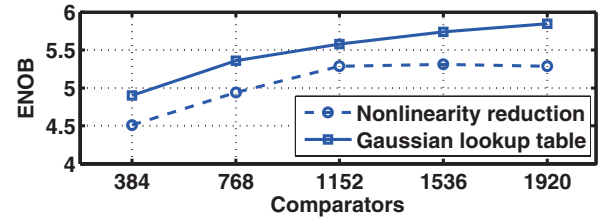
(a) (b)

Fig. 5. a) Die photo. Die dimensions are 2.4mm by 2.4mm. b) Layout screen capture showing detail of functional blocks. Note comparator size in relationship to full adders.

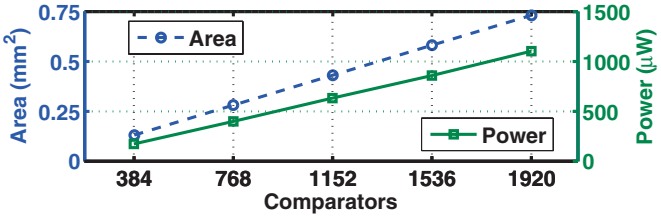
a secondary latch so that the digital output is maintained even when the comparator is reset. The comparator and secondary latch are made with minimum sized devices and incorporated into a digital cell that is comparable in size to a single full adder (Fig. 4). The comparator cell has supply rails that match the pitch of the digital library rails to allow for automated synthesis. This design in fact was not synthesized, but was implemented in this manner for future work.

C. Digital Addition Tree

To perform the digital sum of all of the comparator outputs for each group, a pipelined ripple-carry adder tree was implemented. Each comparator output is a single digital bit that is added with its two nearest neighbors with a 1-bit adder. The 2-



(a)



(b)

Fig. 6. a) Measured ENOB plotted against number of comparators activated. The dashed line uses the Gaussian nonlinearity reduction technique described in this paper. For comparison, the solid line is measured ENOB from a single group of comparators using a generated lookup table. b) Area and power scale linearly with the number of active comparators.

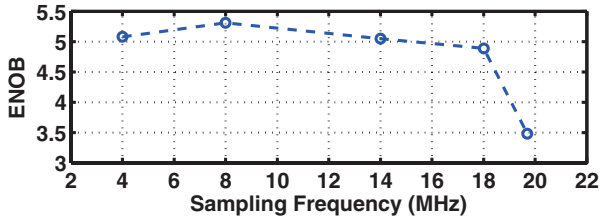
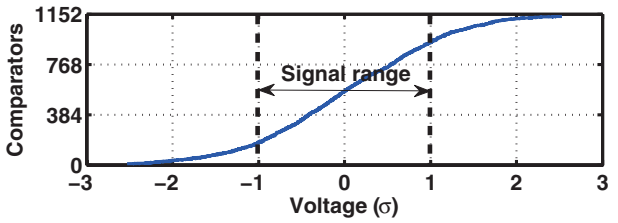


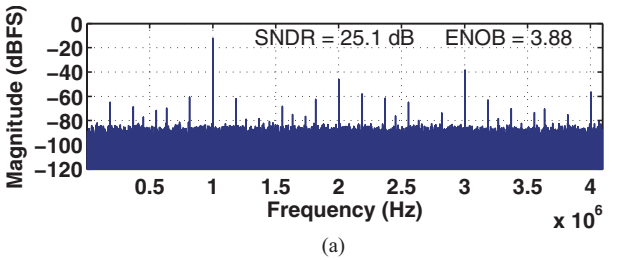
Fig. 7. ENOB plotted against sampling frequency for 1152 comparators configured as described by Fig. 2. f_{in} = 1 MHz and V_{DD} = 900 mV.

bit result is then added with a neighboring 2-bit result to yield a 3-bit result. This continues until finally there is a single 12-bit digital result. Adder stages are separated by d-flip-flops to pipeline the addition in order to minimize the time required for the adder tree to resolve each clock cycle. This architecture was chosen over a Wallace tree because of its highly regular structure in order to simplify implementation.

III. Measurement Results

A test chip was fabricated in 0.18μm CMOS (Fig. 5) with a total area of 5.76 mm^2. It can be seen in Fig. 6(a) that increasing the number of active comparators yields a measured increase in ENOB calculated from SNDR. As a point of reference, comparators are configured as a single group and measured data is multiplied by the inverse of the CDF by a lookup table. This indicates that linearity continues to increase as a function of the number of comparators; however, note that enabling more than 1152 comparators for Gaussian nonlinearity reduction (Fig. 2) does not yield any additional observed improvement. Since area and power scale linearly with the number of comparators (Fig. 6(b)), it was chosen to enable only 1152 comparators to demonstrate the concept and





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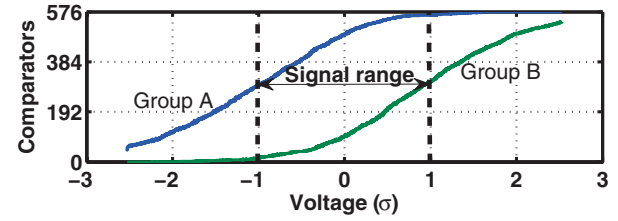

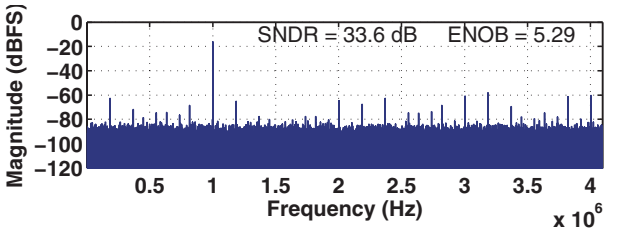

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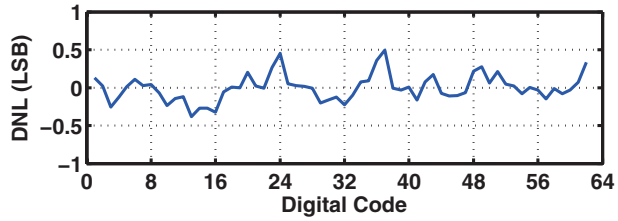

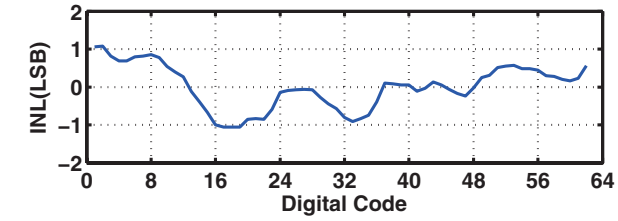

(c)

Fig. 8. a) Measured transfer function of a single group of 1152 parallel comparators ($\sigma \approx$ 140 mV) and FFT of 1 MHz sine input. f_S = 8 MHz. b) Measured transfer function of same parallel comparators as two groups of 576 with differing fixed references set to $-\sigma$ and $+\sigma$ for groups A and B, respectively. Also, FFT of output from the sum of groups A and B of 1 MHz sine input. f_S = 8 MHz. c) DNL and INL of summed output from groups A and B, f_S = 8 MHz.

TABLE I
PERFORMANCE SUMMARY

Technology	0.18μm CMOS
Resolution	6b
Max Sampling Rate	18MS/s
Supply Voltage	900 mV
Comparator Offset Standard Deviation	140 mV
Input Range	280 mVpp (differential)
SNDR / SFDR @ f_S=8 MHz f_{in}=1 MHz	33.59 dB / 42.86 dB
DNL @ f_S=8 MHz	-0.38 / +0.50 LSB
INL @ f_S=8 MHz	-1.06 / +1.07 LSB
Analog Power @ f_S=8 MHz	182μW
Digital Adder Power @ f_S=8 MHz	261μW
Clock Driver Power @ f_S=8 MHz	188μW
Total Power @ f_S=8 MHz	631μW
Core Active Area	0.43 mm^2

obtain additional measurement results; thereby reducing the effective active area to 0.43 mm^2.

Since these digital cell comparators are made up of minimum sized transistors, the standard deviation (σ) of comparator offset is expected to be quite large. In fact, measurement shows that for our test setup with supply voltage of 900 mV, $\sigma \approx$ 140 mV. Because the signal range is $-\sigma$ to $+\sigma$, the resulting signal range is 280 mV. With comparator offsets of this magnitude, it would be difficult to obtain any resolution with conventional circuit techniques. The active comparators are divided into two groups of 576 comparators each and given fixed differential references of $-\sigma$ and $+\sigma$. A 1 MHz sine input is applied and ENOB calculated from SNDR is above 4.9b up to 18MS/s (Fig. 7). The abrupt drop in ENOB observed beyond 18MS/s is due to ripple-carry adders not having enough time to resolve, thus causing gross digital errors. By designing a faster adder tree it should be possible to achieve higher sampling rates.

The Gaussian nonlinearity reduction can be best seen in Fig. 8. With all 1152 comparators acting as a single parallel group, i.e. their inputs are connected and references are connected, sweeping the input with a linear ramp reveals a transfer function that is indeed resemblant of a Gaussian CDF. SNDR of 25.1 dB is achieved with a 1 MHz input and sampling frequency of 8.192 MHz. Using the exact same comparators under the same conditions, but merely dividing them into two groups with differing references, an 8.5 dB improvement in SNDR can be seen. Plots of differential nonlinearity (DNL) and integral nonlinearity (INL) for this test setup can be seen in Fig. 8(c).

Power consumption for the analog portion is 182μW. Digital power is scaled to reflect the amount that is related to the number of active comparators. Digital power consumed by disabled portions of the chip is not included. Digital power is then found to be 449μW with 188μW consumed by clock drivers, leaving 261μW consumed by the pipelined ripple-carry adder tree.

IV. CONCLUSION

A stochastic flash ADC was presented. Using minimum sized comparators that are implemented as digital cells produces a large variation of comparator offset. Typically considered a disadvantage, this large standard deviation of offset is used to set the trip point of each comparator. These trip points are experimentally verified to follow the nonlinear transfer function described by a Gaussian cumulative density function. A technique was presented that can easily reduce this nonlinearity by simply offsetting the references of two comparator groups.

The use of digital cell comparators leads this design to be a good candidate for a highly scaleable and synthesizable ADC. Due to the fact that the signal input range depends on the standard deviation of comparator offset, it may be best suited to serve as the secondary ADC in a fully passive subranging flash, where regular sized comparators resolve the MSBs until the signal is within the range of the stochastic ADC which resolves the LSBs. There would be no need for offset cancellation or computationally intensive calibration and design cost would be reduced if the back end is automatically synthesized.

A test chip was fabricated in 0.18μm CMOS. The test chip achieves over 4.9b ENOB up to 18MS/s with 900mV supply. With a sampling frequency of 8.192 MHz and 1 MHz input, 33.6 dB SNDR is achieved while consuming 631μW and occupying 0.43 mm^2.

ACKNOWLEDGMENT

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